IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Currently amended) A data processing system, comprising:

an interrupt unit~~, wherein the interrupt unit receives~~ for receiving a signal for initiating an interrupt, ~~; and wherein~~ the interrupt unit comprising a plurality of counters for counting ~~counts~~ the occurrence of a plurality of different types of interrupts by interrupt type; and

a storage for storing a count value of each of the plurality of interrupt types.

2. (Currently amended) The data processing system of claim 1, wherein the storage comprises an interrupt descriptor table that associates each interrupt with a corresponding interrupt handler, the interrupt descriptor table storing a count value of an interrupt type ~~is stored~~ in an entry of [[~~an~~]] the interrupt descriptor table.

3. (Currently amended) The data processing system of claim 1, wherein the storage comprises an interrupt count table outside of an interrupt descriptor table of the system, the interrupt count table storing a count value of an interrupt type ~~is stored~~ in an entry of [[~~an~~]] the interrupt count table.

4. (Currently amended) [[~~The~~]] A data processing system ~~of claim 3~~, comprising:

an interrupt unit;

wherein the interrupt unit receives a signal for initiating an interrupt; and

wherein the interrupt unit counts the occurrence of interrupts by type, a count value of an interrupt type being stored in an entry of an interrupt count table, wherein a count offset in an interrupt descriptor table corresponds to the interrupt type.

5. (Original) The data processing system of claim 4, wherein the count offset in the interrupt descriptor table is used to derive an offset address, corresponding to the count value of the interrupt type, in the interrupt count table.

6. (Currently amended) [[The]] A data processing system ~~of claim 3~~, ~~further~~ comprising:

an interrupt unit;

wherein the interrupt unit receives a signal for initiating an interrupt; and

wherein the interrupt unit counts the occurrence of interrupts by type, a count value of an interrupt type being stored in an entry of an interrupt count table; and

a register having a pointer to a memory address of the interrupt count table.

7. (Currently amended) The data processing system of claim 1, ~~further comprising~~ wherein the plurality of counters comprise hardware counters that count the occurrence of interrupts by type.

8. (Original) The data processing system of claim 1, wherein the types of interrupts include TLB (translation lookaside buffer) fault and VHPT (virtual hash page table) Instruction fault.

9. (Original) The data processing system of claim 1, wherein when a count is about to overflow, an overflow signal is sent.

10. (Currently amended) A method for executing instructions on an information processing system, comprising the steps of:

receiving an interrupt signal at an interrupt unit, wherein the interrupt signal is for initiating an interrupt in a processor;

responsive to receiving the interrupt signal, incrementing a first counter of a plurality of counters based on a type of interrupt among a plurality of types of interrupts associated with the interrupt signal;

~~wherein the first counter is one of a plurality of counters; and~~

wherein the plurality of counters counts the occurrence of interrupts by type of interrupt.

11. (Currently amended) The method of claim 10, and further comprising storing ~~wherein~~ a count value of the first counter ~~is stored~~ in an entry of an interrupt descriptor table that associates each interrupt with a corresponding interrupt handler.

12. (Currently amended) The method of claim 10, and further comprising storing ~~wherein~~ a count value of an interrupt type ~~is stored~~ in an entry of an interrupt count table outside of an interrupt descriptor table of the system.

13. (Currently amended) [[~~The~~]] A method ~~of claim 12,~~ for executing instructions on an information processing system, comprising the steps of:

receiving an interrupt signal at an interrupt unit, wherein the interrupt signal is for initiating an interrupt in a processor;

responsive to receiving the interrupt signal, incrementing a first counter based on a type of interrupt associated with the interrupt signal;

wherein the first counter is one of a plurality of counters; and

wherein the plurality of counters counts the occurrence of interrupts by type, a count value of an interrupt type being stored in an entry of an interrupt count table; and wherein a count offset in an interrupt descriptor table corresponds to the interrupt type.

14. (Original) The method of claim 13, wherein the count offset in the interrupt descriptor table is used to derive an offset address, corresponding to the count value of the interrupt type, in the interrupt count table.

15. (Currently amended) [[The]] A method ~~of claim 12,~~ for executing instructions on an information processing system, comprising the steps of:

receiving an interrupt signal at an interrupt unit, wherein the interrupt signal is for initiating an interrupt in a processor;

responsive to receiving the interrupt signal, incrementing a first counter based on a type of interrupt associated with the interrupt signal;

wherein the first counter is one of a plurality of counters; and

wherein the plurality of counters counts the occurrence of interrupts by type, a count value of an interrupt type being stored in an entry of an interrupt count table; and further comprising:

a register having a pointer to a memory address of the interrupt count table.

16. (Currently amended) The method of claim 10, wherein the counters of the plurality of counters are hardware counters.

17. (Original) The method of claim 10, wherein the types of interrupts include TLB (translation lookaside buffer) fault and VHPT (virtual hash page table) Instruction fault.

18. (Original) The method of claim 10, wherein when a count is about to overflow, an overflow signal is sent.

19. (Currently amended) A computer program product in a computer readable medium, comprising:

first instructions for receiving an interrupt signal [[~~from~~]] at an interrupt unit for initiating an interrupt in a processor;

second instructions for, responsive to receiving the interrupt signal, incrementing a first counter of a plurality of counters based on a type of interrupt among a plurality of types of interrupts associated with the interrupt signal;

~~wherein the first counter is one of a plurality of counters; and~~

wherein the plurality of counters counts the occurrence of interrupts by type of interrupt.

20. (Currently amended) The computer program product of claim 19, and further comprising instructions for storing ~~wherein~~ a count value of an interrupt type ~~is stored~~ in an entry of an interrupt descriptor table that associates each interrupt with a corresponding interrupt handler.

21. (Currently amended) The computer program product of claim 19, and further comprising instructions for storing ~~wherein~~ a count value of an interrupt type ~~is stored~~ in an entry of an interrupt count table outside of an interrupt descriptor table of the system.

22. (Currently amended) [[The]] A computer program product ~~of claim 21,~~ in a computer readable medium, comprising:

first instructions for receiving an interrupt signal at an interrupt unit for initiating an interrupt in a processor;

second instructions for, responsive to receiving the interrupt signal, incrementing a first counter associated with the interrupt signal;

wherein the first counter is one of a plurality of counters;

wherein the plurality of counters counts the occurrence of interrupts by type, a count value of an interrupt type being stored in an entry of an interrupt count table,

wherein a count offset in an interrupt descriptor table corresponds to an interrupt type.

23. (Original) The computer program product of claim 22, wherein the count offset in the interrupt descriptor table is used to derive an offset address, corresponding to the count value of an interrupt type, in the interrupt count table.

24. (Currently amended) [[~~The~~]] A computer program product ~~of claim 21,~~ in a computer readable medium, comprising:

first instructions for receiving an interrupt signal at an interrupt unit for initiating an interrupt in a processor;

second instructions for, responsive to receiving the interrupt signal, incrementing a first counter associated with the interrupt signal;

wherein the first counter is one of a plurality of counters;

wherein the plurality of counters counts the occurrence of interrupts by type, a count value of an interrupt type being stored in an entry of an interrupt count table; and further comprising:

a register having a pointer to a memory address of the interrupt count table.

25. (Currently amended) The computer program product of claim 19, wherein the counters of the plurality of counters are hardware counters.

26. (Original) The computer program product of claim 19, wherein the types of interrupts include TLB (translation lookaside buffer) fault and VHPT (virtual hash page table) Instruction fault.

27. (Original) The computer program product of claim 19, wherein when a count is about to overflow, an overflow signal is sent.